

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Rule 53(b) Divisional Application of S.N. 08/970,212:

Shunji NAKAMURA

Serial No.: NEW

Group Art Unit: **2811** (Expected)

Filed: **December 6, 2001**

Examiner: **NADAV, O.** (Expected)

For: **SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING
THE SAME**

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

December 6, 2001

Sir:

Prior to calculation of the filing fee and examination of this application, please amend the
above-identified application as follows:

IN THE CLAIMS:

Please **ADD** the following new claims 29-31:

29. (New) A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed

therein and having substantially flat surfaces, said silicon layer defining a first side and a second

side;

6 a gate electrode formed only on said first side of the silicon layer between the first
7 diffused region and the second diffused region interposing a gate insulating film between the gate
8 electrode and the silicon layer;

9 a contact electrode formed on said first side of the silicon layer and connected to the
10 second diffused region; and

11 a capacitor formed only on said first side of the silicon layer and having a storage
12 electrode connected to the first diffused region;

13 a bit line formed on said second side of the silicon layer and electrically connected to the
14 second diffused region via the contact electrode;

15 a support substrate formed on said first side of the silicon layer for supporting the device
16 layer interposing an insulating film between the support substrate and the device layer; and

17 a strapping word line formed on said second side of the silicon layer and connected to the
18 gate electrode.

1 30. (New) A semiconductor memory device comprising:

2 a device layer including:

3 a silicon layer having a first diffused region and a second diffused region formed
4 therein and having substantially flat surfaces, said silicon layer defining a first side and a second
5 side;

6 a gate electrode formed only on said first side of the silicon layer between the first
7 diffused region and the second diffused region interposing a gate insulating film between the gate
8 electrode and the silicon layer;

9 a contact electrode formed on said first side of the silicon layer and connected to the
10 second diffused region; and

11 a capacitor formed only on said first side of the silicon layer and having a storage
12 electrode connected to the first diffused region;

13 a bit line formed on said second side of the silicon layer and electrically connected to the
14 second diffused region via the contact electrode;

15 a support substrate formed on said first side of the silicon layer for supporting the device
16 layer interposing an insulating film between the support substrate and the device layer; and

17 a strapping word line formed on said first side of the silicon layer and connected to the gate
18 electrode.

1 31. (New) A semiconductor memory device comprising:

2 a device layer including:

3 a silicon layer having a first diffused region and a second diffused region formed
4 therein and having substantially flat surfaces, said silicon layer defining a first side and a second
5 side;

6 a gate electrode formed only on said first side of the silicon layer between the first
7 diffused region and the second diffused region interposing a gate insulating film between the gate
8 electrode and the silicon layer;

9 a contact electrode formed on said first side of the silicon layer and connected to the
10 second diffused region; and

11 a capacitor formed only on said first side of the silicon layer and having a storage
12 electrode connected to the first diffused region;

13 a bit line formed on said second side of the silicon layer and electrically connected to the
14 second diffused region via the contact electrode;

15 a support substrate formed on said first side of the silicon layer for supporting the device
16 layer interposing an insulating film between the support substrate and the device layer; and

17 a shield electrode formed above the bit line for suppressing interference between the bit lines.

REMARKS

The above amendment to the claims has been made to put the application in better condition for examination.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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